REMARKS

The present response amends the abstract. No claims have been amended or canceled. Claims 1-21 remain pending in the captioned case. Further examination and reconsideration of the present application are respectfully requested.

Objection to Abstract

An objection was lodged against the abstract for an informality. Specifically, the Examiner objected to the length of the abstract as exceeding 150 words. In response thereto, the abstract has been amended to obviate this objection.

Section 102 Rejection

Claims 1-7 and 11-21 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,553,525 to Shephard, III (hereinafter "Shephard"). The standard for "anticipation" is one of fairly strict identity. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art of reference. *Verdegaal Bros. v. Union Oil Co. of California*, 2 USPQ 2d. 1051, 1053 (Fed. Cir. 1987); MPEP 2131. Applicants submit that Shephard fails to disclose each and every element of the currently pending claims. Some distinctive features of the independent claims are set forth in more detail below. However, it is understood that in addition to differences between Shephard and the independent claims, there are also numerous differences between Shephard and dependent claims. Initially, however, Applicants believe distinctions over the independent claims are more than adequate to impart patentability to the captioned application.

Shephard does not teach or suggest a data control register comprising a plurality of select bits corresponding to a plurality of memory devices. Claim 1 makes clear that a singular data control register comprises a plurality of select bits. Moreover, the select bits within the data control register corresponds to a plurality of memory devices. If one of the plurality of select bits is set that corresponds to a particular memory device, then that memory device is "write access enabled." On page 3 of the Office Action, allegation was made that Shephard discloses a plurality of memory devices 102, 104, 106, and 108, shown in Fig. 1 of Shephard as separately controllable arrays (Shephard – Fig. 1). The Office Action also alleges

that Shephard discloses a data control register 308 that comprises a plurality of select bits (D+1 bits) (Shephard – Fig. 3)

Contrary to present claim 1, Shephard makes clear that the D number of bits within the control register 308 "is equal to the width of array 310." (Shephard – col. 4, lines 14-16.) Instead of D bits corresponding to a plurality of memory devices (defined in the Office Action as arrays 102, 104, 106, and 108), the D bits correspond to D number of rows within a single array 310. Thus, Shephard does not teach or suggest a single data control register having a plurality of select bits corresponding to a plurality of memory devices. In addition, Shephard and does not suggest write access enabling one of the plurality of memory devices (i.e., device 102 versus device 104) if a corresponding one of the plurality of select bits is set. Thus, Shephard does not teach or suggest, nor can Shephard be modified to teach or suggest, the claimed data control register having select bits corresponding to each of a particular one of a plurality of memory devices, such as memory devices 102, 104, 106, and 108 of Shephard.

Shephard does not teach or suggest a control register comprising a plurality of control bits corresponding to the plurality of memory devices (claim 1); or each of the plurality of control bits corresponding to a specific one of the plurality of memory devices (claim 13). Similar to the shortcomings of Shephard related to the data control register with select bits corresponding to each of a plurality of memory devices, Shepard also does not suggest a control register having a plurality of control bits corresponding to each of a plurality of memory devices. The Office Action alleges on page 3 that control register 302 in Shephard comprises a plurality of control bits corresponding to the plurality of memory devices as claimed. Applicants disagree.

First, control register 302 does not comprise a plurality of control bits corresponding to the plurality of memory devices. As set forth in present claim 1, the plurality of memory devices refers to the same plurality of memory devices write-access enabled by the select bits within the data control register. While Shephard illustrates select bits D enabling portions of a single array (not one of a plurality of arrays), Shephard in no way suggests that control register 302 also enables control bits corresponding to the same plurality of memory devices write access enabled by the data control register 308. Simply put, control register 302 and data control register 308 of Shephard contain bits destined to control or select a mutually exclusive plurality of memory devices – not the same plurality of memory devices as claimed (*See,* Shephard – Fig. 3 referencing pointer control registers as controlling instruction array 300 versus data control registers 308 controlling accesses to array 310, separate and apart from array 300.)

Shepard does not teach or suggest copying control bits to select bits (claims 1 and 13). Since pointer control register 302 contains altogether different bits (i.e., pointer control bits) than the separate row selection bits D within data control register 308, Shephard not only teaches the difference between control register bits and data register bits, but makes clear to a skilled artisan that the bits must be dissimilar and, thus, cannot be copied from the control register to the data register as claimed (Shephard -- Fig. 3; col. 3, line 60 - col. 4, line 22). Thus, not only does Shephard fail to teach or suggest copying control bits within its control register 302 to select bits within its data control register 308, but purposely teaches away from any form of copying since the control bits are destined for selection of a separate array (array 300) from the select bits destined for array 310. The bits within registers 302 and 308 are chosen for an entirely different purpose than the present claimed invention; thus, there cannot be any form of copying from register 302 to register 308 since to do so would defeat the purpose of Shephard that requires use of bits within register 302 and register 308 to be different, not "shadowing" each other as claimed.

With respect to independent claim 20 and dependent claim 21, the Office Action provides a blanket assertion that these claims were rejected "under the same rationale as discussed above . . ." Although independent claim 20 is considerably different than, and must be construed separate from, independent claims 1 and 13 under the doctrine of claim differentiation, the Office Action nonetheless provides no insights as to why independent claim 20 must be rejected under the same rationale as independent claims 1 and 13, or any claims dependent therefrom. Thus, absent any allegations specifically pertinent to claim 20, Applicants traverse this rejection for the same rationale stated above for independent claims 1 and 13. However, Applicants invite the Examiner to provide any reference that would teach or suggest operating a second set of bits solely from a host processor link coupled to but external from a monolithic substrate containing a set of memory devices, as set forth in present claim 20.

For at least the reasons stated above, Applicants assert that independent claims 1, 13, and 20, as well as claims dependent therefrom, are not anticipated by the cited art. Accordingly, Applicants respectfully request removal of this rejection.

Section 103 Rejection

Claims 8-9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Shephard. To establish a case of *prima facie* obviousness of a claimed invention, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the

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knowledge generally available to one of ordinary skill in the art. Second, there must be a reasonable expectation of success. As stated in MPEP 2143.01, the fact that references can be hypothetically combined or modified is not sufficient to establish a *prima facie* case of obviousness. *See In re Mills*, 916 F.2d. 680 (Fed. Cir. 1990). Finally, the prior art references must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d. 981 (CCPA 1974); MPEP 2143.03. Specifically, "all words in a claim must be considered when judging the patentability of that claim against the prior art." *In re Wilson* 424 F.2d., 1382 (CCPA 1970). Using these standards, Applicants contend that the cited art fails to teach or suggest all features of the currently pending claims.

As stated above, Shephard does not teach or suggest a control register comprising a plurality of control bits, nor does Shephard teach or suggest a data control register comprising a plurality of select bits. Absent the claimed control register or data control register set forth in independent claim 1, Shephard cannot suggest the combination of independent claim 1, with dependent claims 8-10. Nowhere in Shephard is there any reference to direct memory access controller, nor is there any suggestion in Shephard of a host processor interface interposed between a host processor and secondary processors. In fact, absent the generic term "processor" used in the abstract, there is no demarcation or suggestion thereof in Shephard of a host processor being separate and apart from secondary processors, or DMA controllers associated with each of a plurality of secondary processors as set forth in dependent claims 8-10.

While it is permissible for an Examiner to take Official Notice as to certain concepts and advantages for having DMA controllers and secondary processors as claimed, it is impermissible for an Examiner to take Official Notice or reference to any form of implicit disclosure absent some suggestion within Shephard itself that would lead a person skilled in the art to combine DMA controllers and secondary processors into the teachings of Shephard to arrive at the present claims. In accordance with MPEP 2144.03, "if the applicant traverses such an assertion, the Examiner should cite a reference in support of his or her position." Applicants hereby traverse the Examiner's position of Official Notice, and request the Examiner to provide facts in support of his position by reference, affidavit, or otherwise with regard to the obviousness rejection on page 5 of the Office Action. *See*, MPEP 2144.03; *In re Malcolm*, 129 F.2d. 529 (CCPA 1942); *In re Boon*, 439 F.2d. 724 (CCPA 1971).

Unless the Examiner can provide the requisite evidence of obviousness or obviousness to combine, Applicants request that this rejection be removed in its entirety.

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CONCLUSION

The present amendment and response is believed to be a complete response to the issues raised in the Office Action mailed March 26, 2004. In view of the remarks traversing the rejections, Applicants assert that pending claims 1-21 are in condition for allowance. If the Examiner has any questions, comments or suggestions, the undersigned earnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees which may be required, or credit any overpayment, to LSI Logic Corp. Deposit Account No. 12-2252/01-545.

Respectfully submitted,

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